FIG. 1

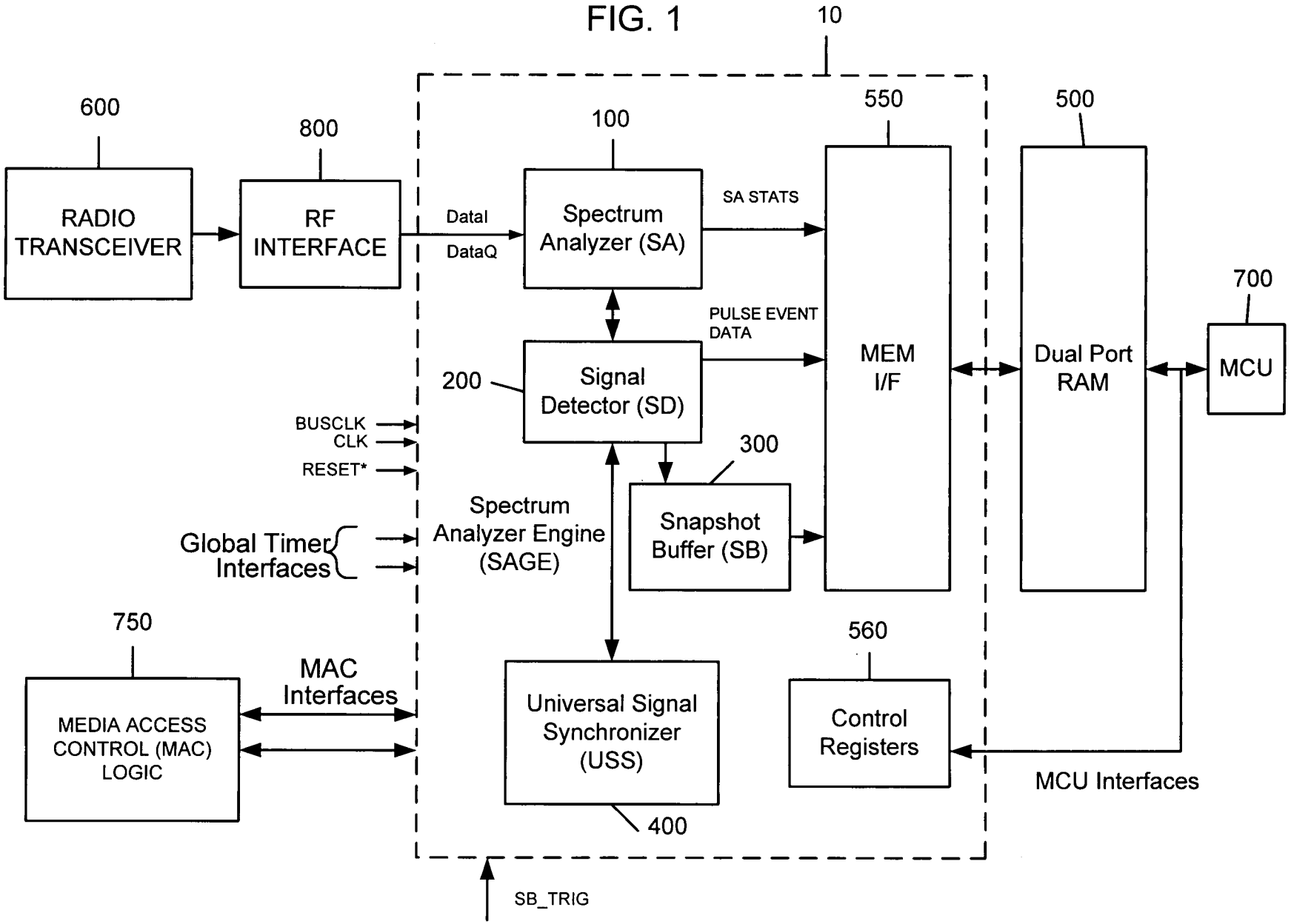

10
600
RADIO TRANSCEIVER
800
RF INTERFACE
Datal
DataQ
100
Spectrum Analyzer (SA)
SA STATS
550
MEM I/F
500
Dual Port RAM
700
MCU
PULSE EVENT DATA
200
Signal Detector (SD)
BUSCLK
CLK
RESET*
300
Snapshot Buffer (SB)
Spectrum Analyzer Engine (SAGE)
Global Timer Interfaces
750
MAC Interfaces
MEDIA ACCESS CONTROL (MAC) LOGIC
Universal Signal Synchronizer (USS)
400
560
Control Registers
MCU Interfaces
SB_TRIG

FIG. 2

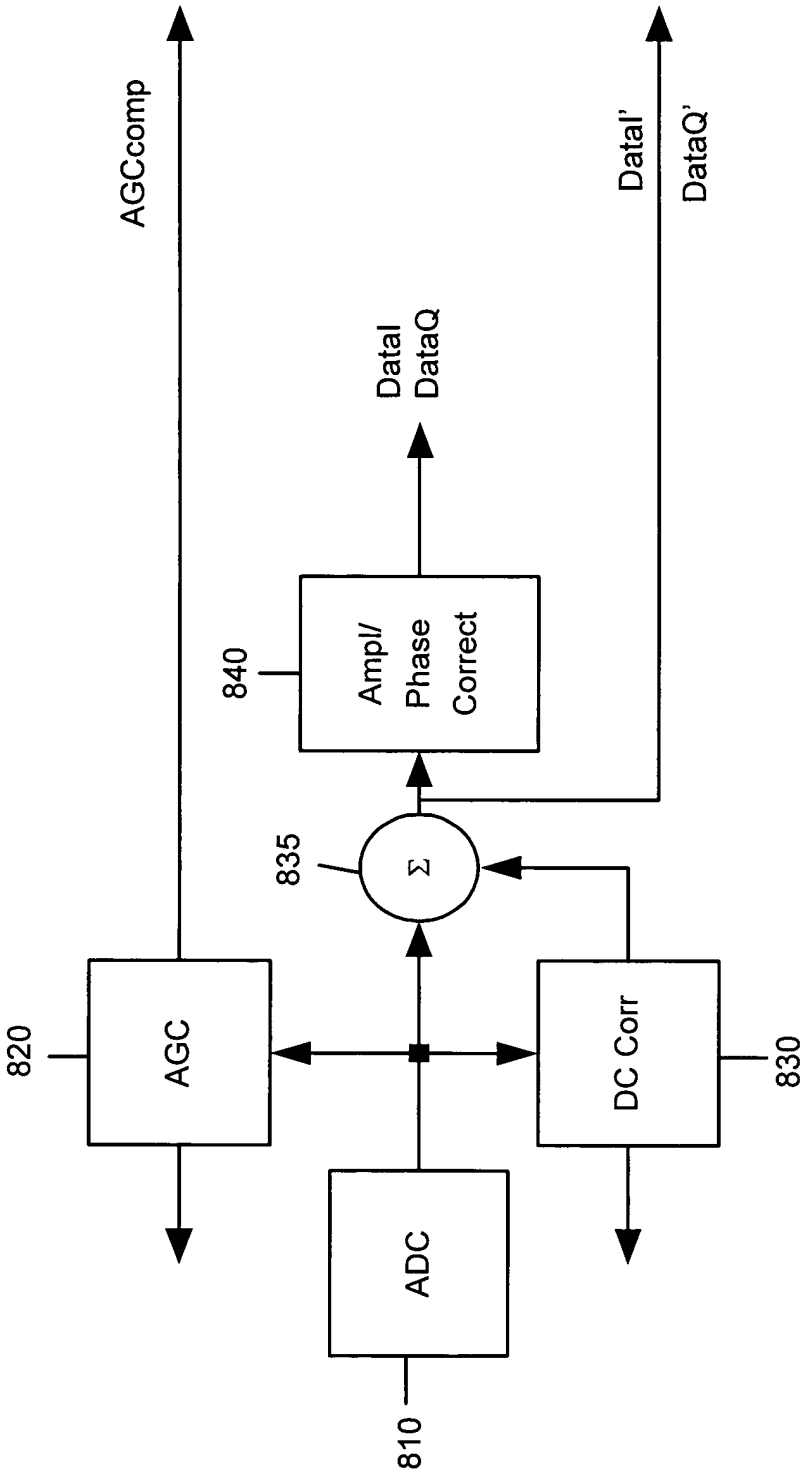

AGCcomp
DataI
DataQ
DataI'
DataQ'
840
Ampl/
Phase
Correct
835
Σ
820
AGC
DC Corr
830
ADC
810

FIG. 3

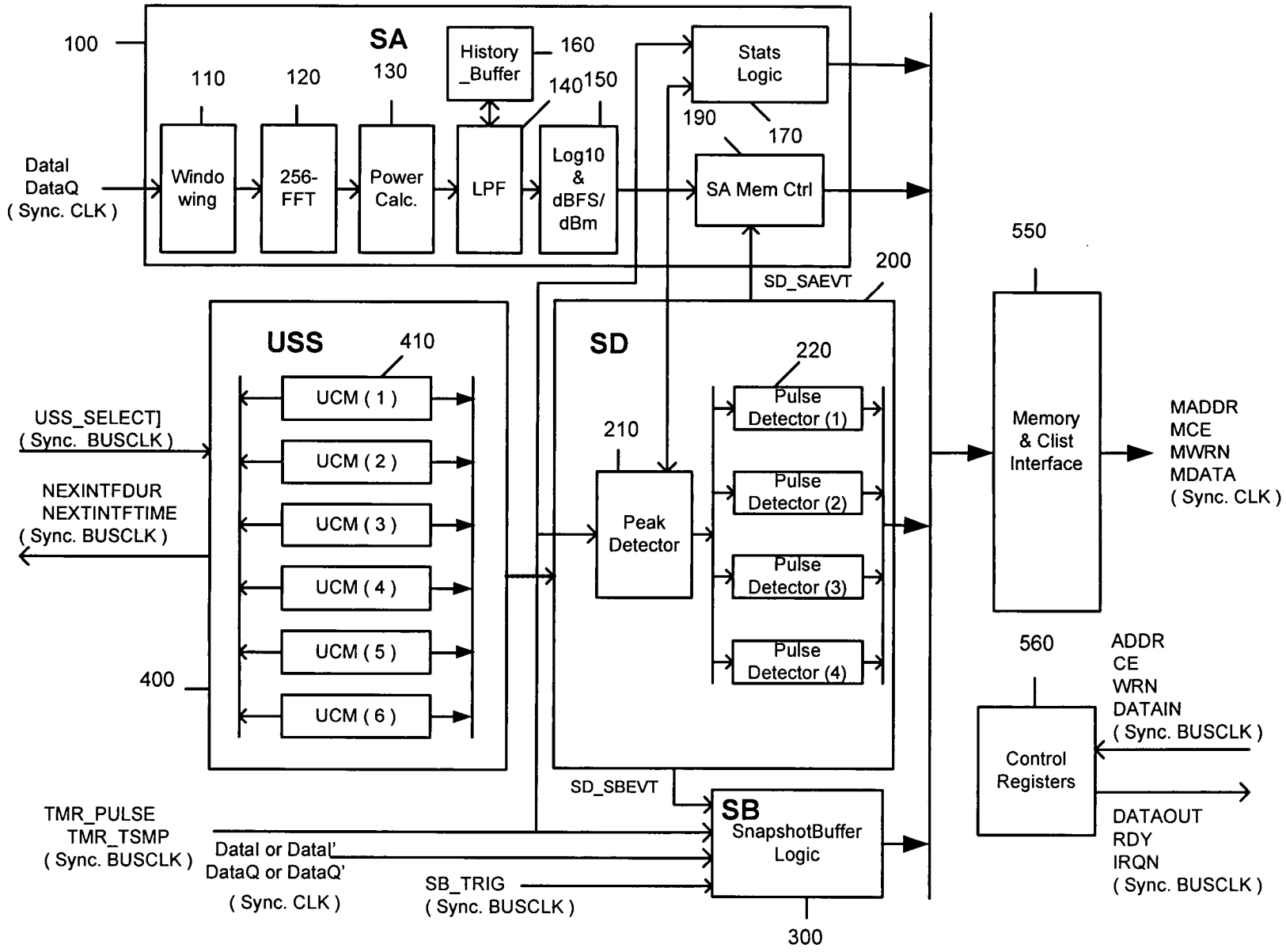

100
SA
110
120
130
History _Buffer
160
140
150
Stats Logic
190
170
SA Mem Ctrl
Datal DataQ (Sync. CLK)
Windo wing
256-FFT
Power Calc.
LPF
Log10 & dBFS/ dBm
SD_SAEVT
200
550
USS
410
SD
220
USS_SELECT] (Sync. BUSCLK)
NEXINTFDUR NEXTINTFTIME (Sync. BUSCLK)
UCM (1)
UCM (2)
UCM (3)
UCM (4)
UCM (5)
UCM (6)
400
210
Peak Detector
Pulse Detector (1)
Pulse Detector (2)
Pulse Detector (3)
Pulse Detector (4)
Memory & Clist Interface
MADDR
MCE
MWRN
MDATA
(Sync. CLK)
560
ADDR
CE
WRN
DATAIN
(Sync. BUSCLK)
Control Registers
DATAOUT
RDY
IRQN
(Sync. BUSCLK)
SD_SBEVT
SB
SnapshotBuffer Logic
TMR_PULSE
TMR_TSMP
(Sync. BUSCLK)
Datal or Datal'
DataQ or DataQ'
(Sync. CLK)
SB_TRIG
(Sync. BUSCLK)
300

FIG. 4

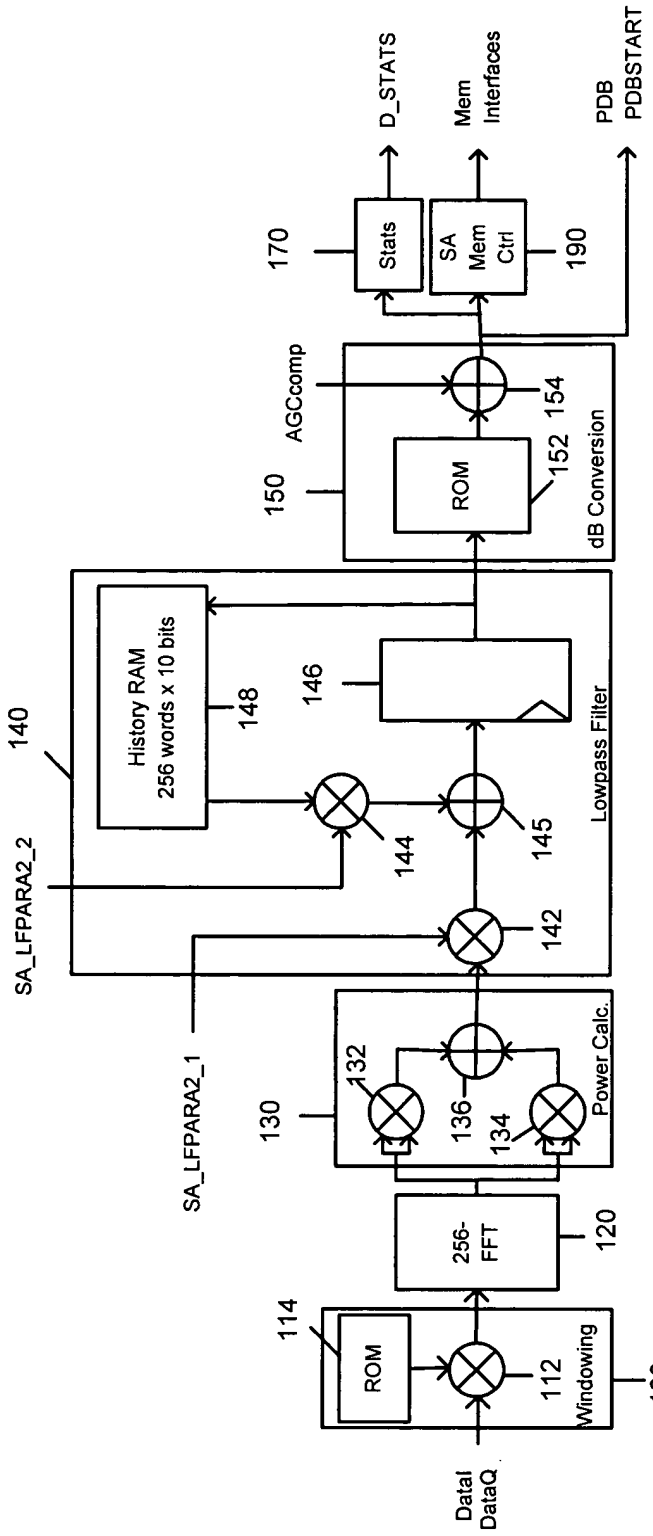

Windowing
ROM
112
114
100
256-FFT
120
Power Calc.
130
132
134
136
SA_LFPARA2_1
Lowpass Filter
140
SA_LFPARA2_2
142
144
145
146
History RAM
256 words x 10 bits
148
dB Conversion
150
AGCcomp
ROM
152
154
170
Stats
SA Mem Ctrl
190
D_STATS
Mem Interfaces
PDB
PDBSTART
DataI
DataQ

FIG. 5

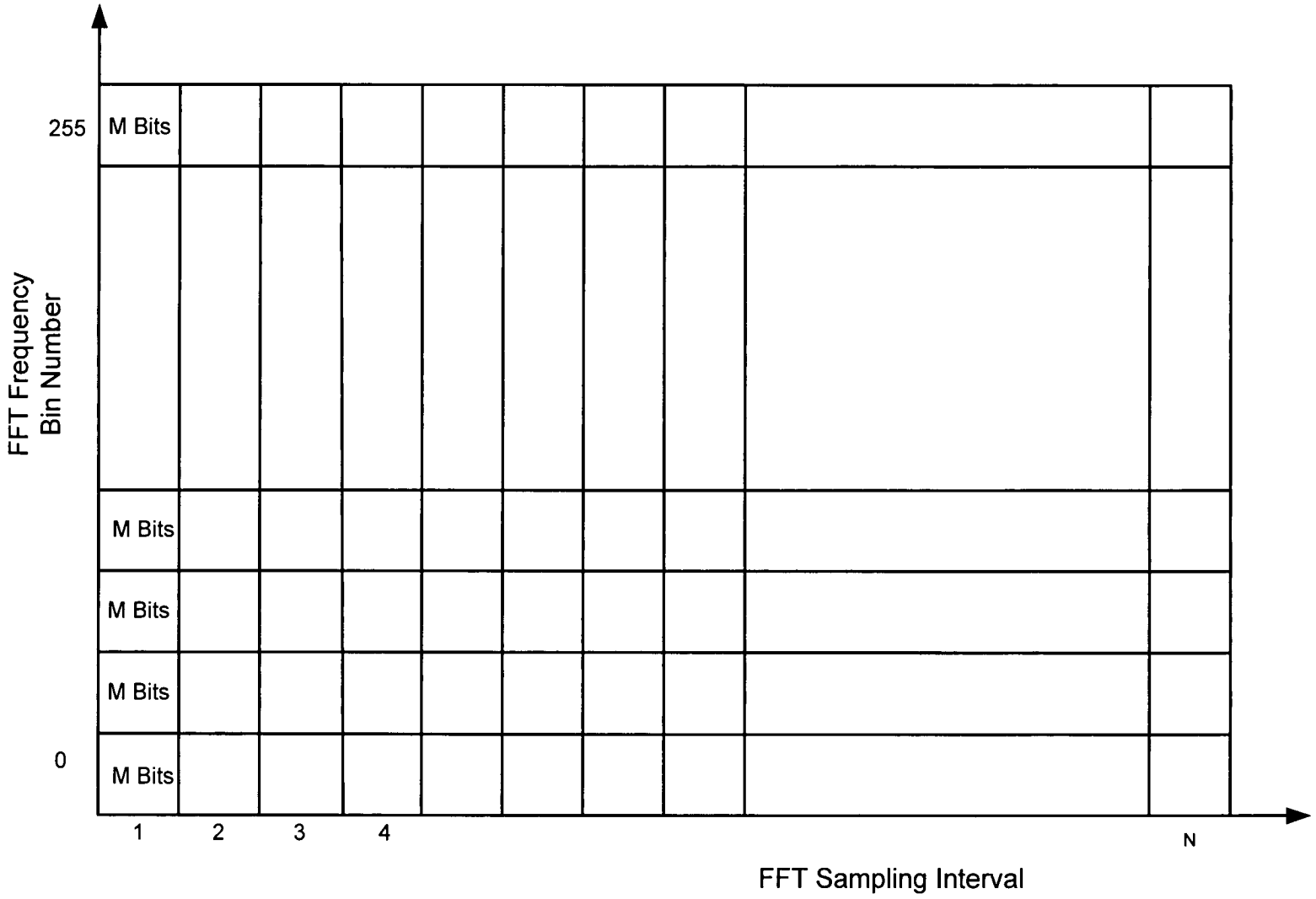

255
M Bits
M Bits
M Bits
M Bits
M Bits
0
FFT Frequency
Bin Number
1
2
3
4
N
FFT Sampling Interval

FIG. 6

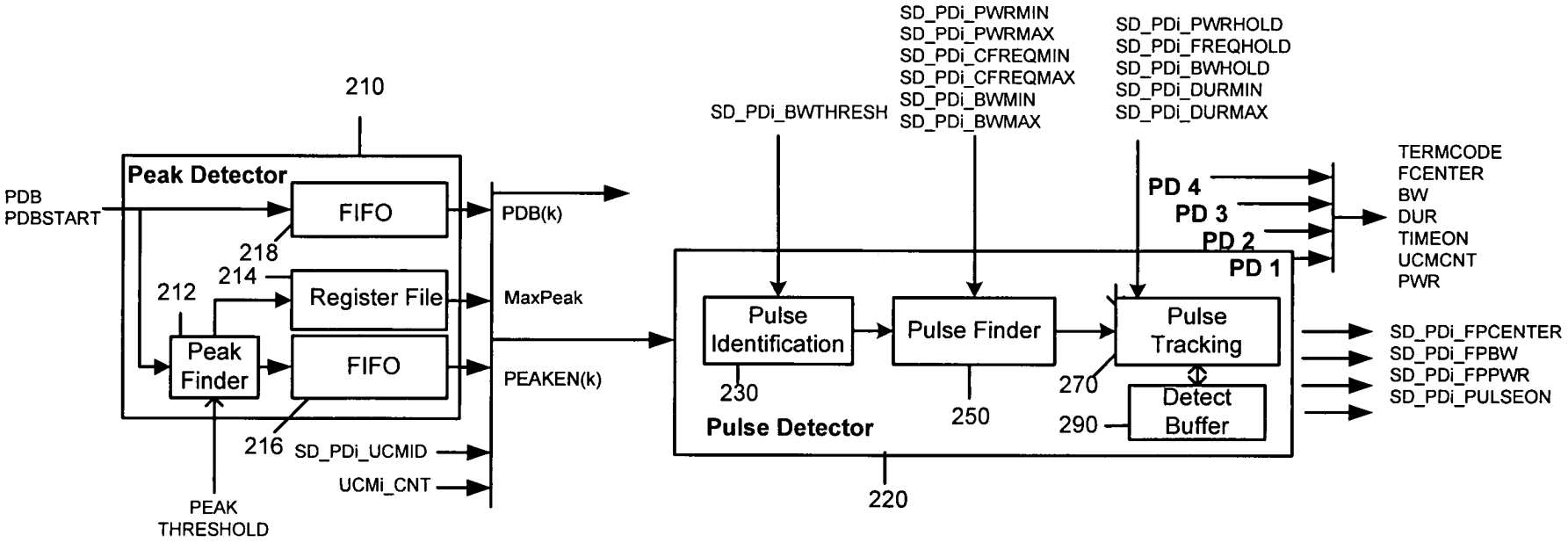

210
Peak Detector
PDB
PDBSTART
FIFO
218
214
212
Register File
Peak
Finder
FIFO
216
PEAK
THRESHOLD
PDB(k)
MaxPeak
PEAKEN(k)
SD_PDi_UCMID
UCMi_CNT
SD_PDi_BWTHRESH
SD_PDi_PWRMIN
SD_PDi_PWRMAX
SD_PDi_CFREQMIN
SD_PDi_CFREQMAX
SD_PDi_BWMIN
SD_PDi_BWMAX
SD_PDi_PWRHOLD
SD_PDi_FREQHOLD
SD_PDi_BWHOLD
SD_PDi_DURMIN
SD_PDi_DURMAX
PD 4
PD 3
PD 2
PD 1
TERMCODE
FCENTER
BW
DUR
TIMEON
UCMCNT
PWR
Pulse
Identification
Pulse Finder
Pulse
Tracking
230
250
270
290
Detect
Buffer
Pulse Detector
220
SD_PDi_FPCENTER
SD_PDi_FPBW
SD_PDi_FPPWR
SD_PDi_PULSEON

FIG. 7

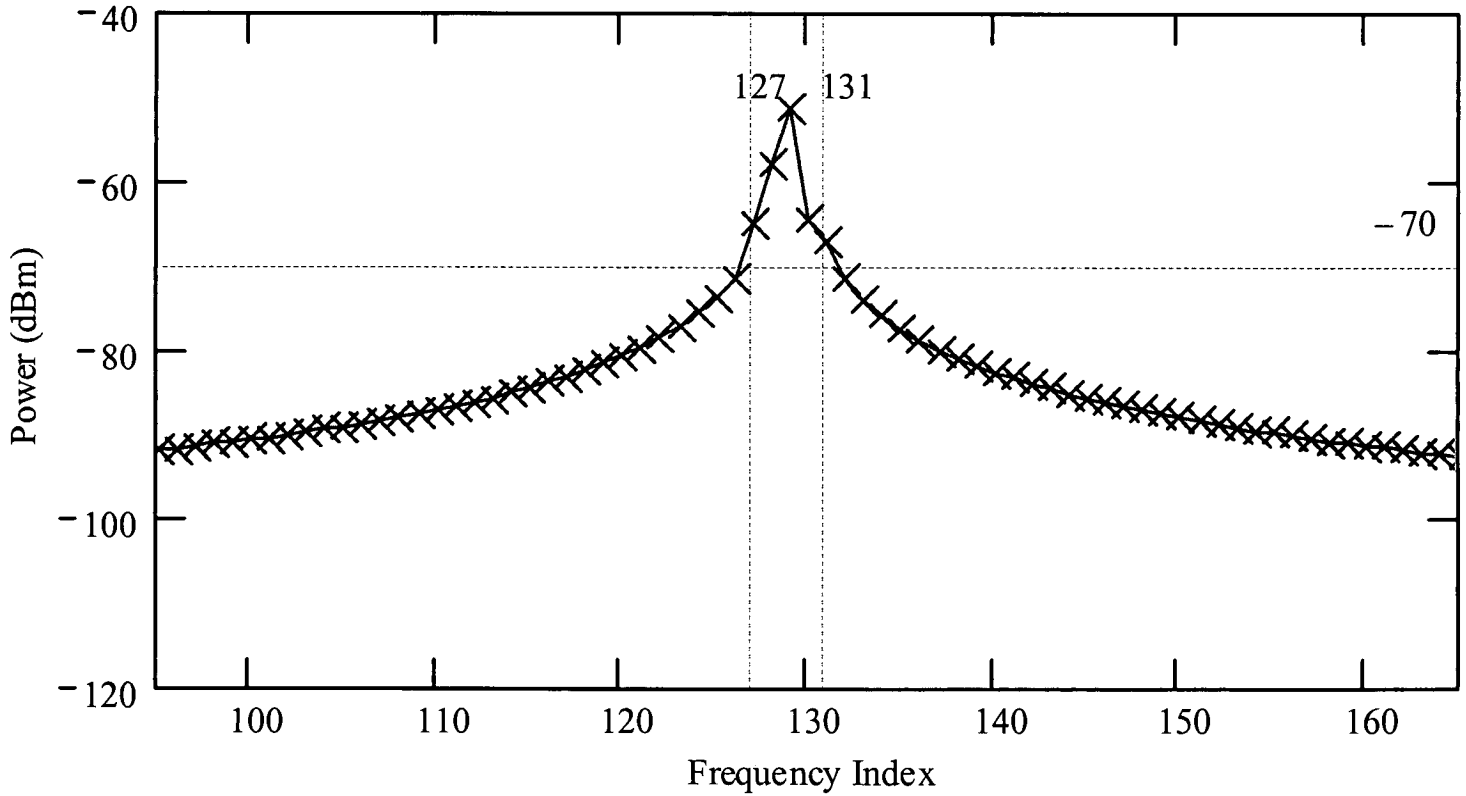

-40
-60
-80
-100
-120
Power (dBm)
127
131
-70
100
110
120
130
140
150
160
Frequency Index

FIG. 8

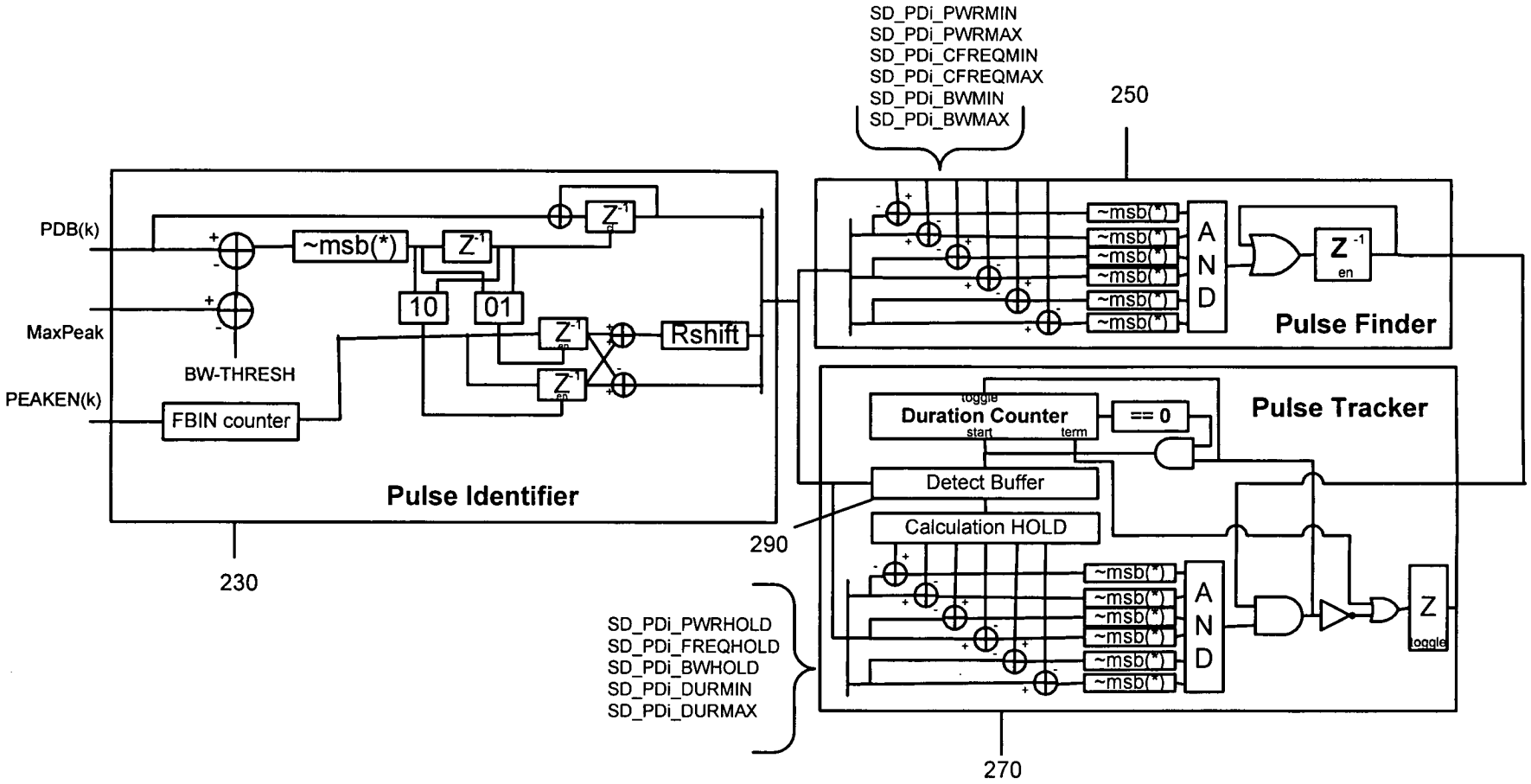

SD_PDi_PWRMIN
SD_PDi_PWRMAX
SD_PDi_CFREQMIN
SD_PDi_CFREQMAX
SD_PDi_BWMIN
SD_PDi_BWMAX
250
PDB(k)
MaxPeak
BW-THRESH
PEAKEN(k)
FBIN counter
~msb(*)
10
01
Rshift
Pulse Identifier
230
AND
Pulse Finder
Pulse Tracker
toggle
Duration Counter
start
term
== 0
Detect Buffer
Calculation HOLD
290
SD_PDi_PWRHOLD
SD_PDi_FREQHOLD
SD_PDi_BWHOLD
SD_PDi_DURMIN
SD_PDi_DURMAX
270

FIG. 9

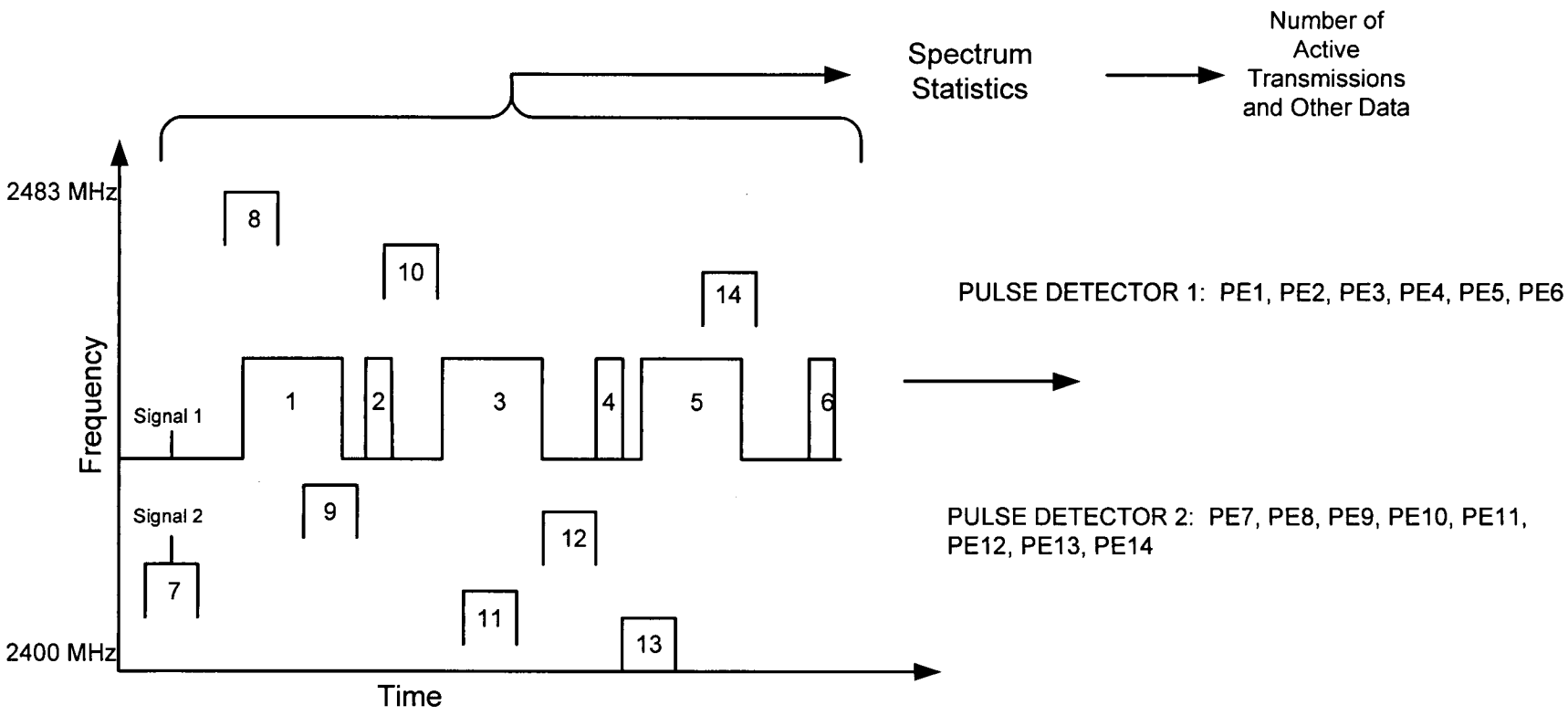

Spectrum Statistics
Number of Active Transmissions and Other Data
2483 MHz
2400 MHz
Frequency
Time
Signal 1
Signal 2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
PULSE DETECTOR 1: PE1, PE2, PE3, PE4, PE5, PE6
PULSE DETECTOR 2: PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14

FIG. 10

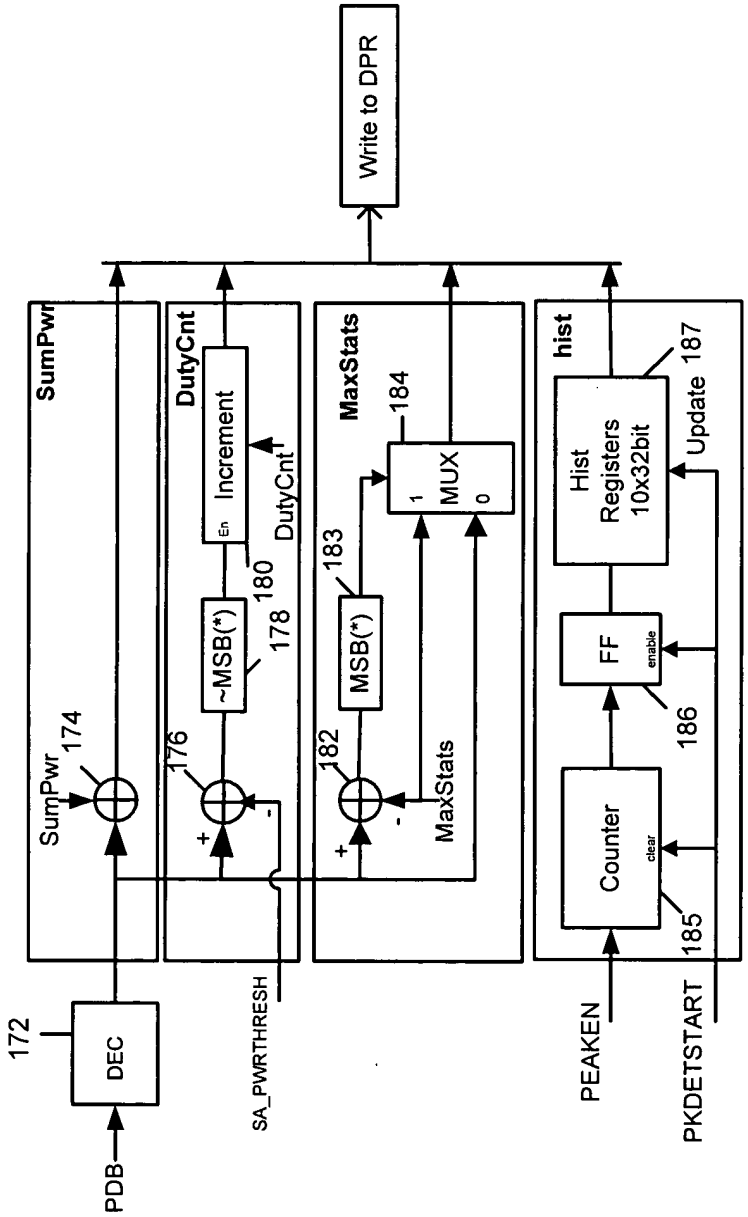

170
SumPwr
DutyCnt
MaxStats
hist
Write to DPR
DEC
172
PDB
SumPwr
174
176
+
-
~MSB(*)
178
Increment
En
DutyCnt
180
SA_PWRTHRESH
MSB(*)
183
182
+
-
MaxStats
MUX
1
0
184
Hist
Registers
10x32bit
Update
187
FF
enable
186
Counter
clear
185
PEAKEN
PKDETSTART

FIG. 11

Time / Freq	0	1	2	3	4	5
0	-100	-100	-50	-50	-50	-50
	-100	-100	-50	-50	-50	-50
20	-100	-100	-50	-50	-50	-50
	-100	-100	-100	-100	-100	-100
125	-100	-100	-30	-30	-30	-30
	-100	-100	-30	-30	-30	-30
175	-100	-100	-30	-30	-30	-30
	-100	-100	-100	-100	-100	-100
200	-100	-100	-100	-50	-50	-50
	-100	-100	-100	-50	-50	-50
255	-100	-100	-100	-50	-50	-50

→

SumPwr	DutyCnt	MaxPwr
-400	4	-50
-400	4	-50
-400	4	-50
-600	0	-100
-320	4	-30
-320	4	-30
-320	4	-30
-600	0	-100
-450	3	-50
-450	3	-50
-450	3	-50

FIG. 12

	Number of Stats Update Cycles With:
No Peaks	2
1 Peak	0
2 Peaks	1
3 Peaks	3
4 Peaks	0
5 Peaks	0
6 Peaks	0
7 Peaks	0
8 Peaks	0
9 Peaks	0

FIG. 13

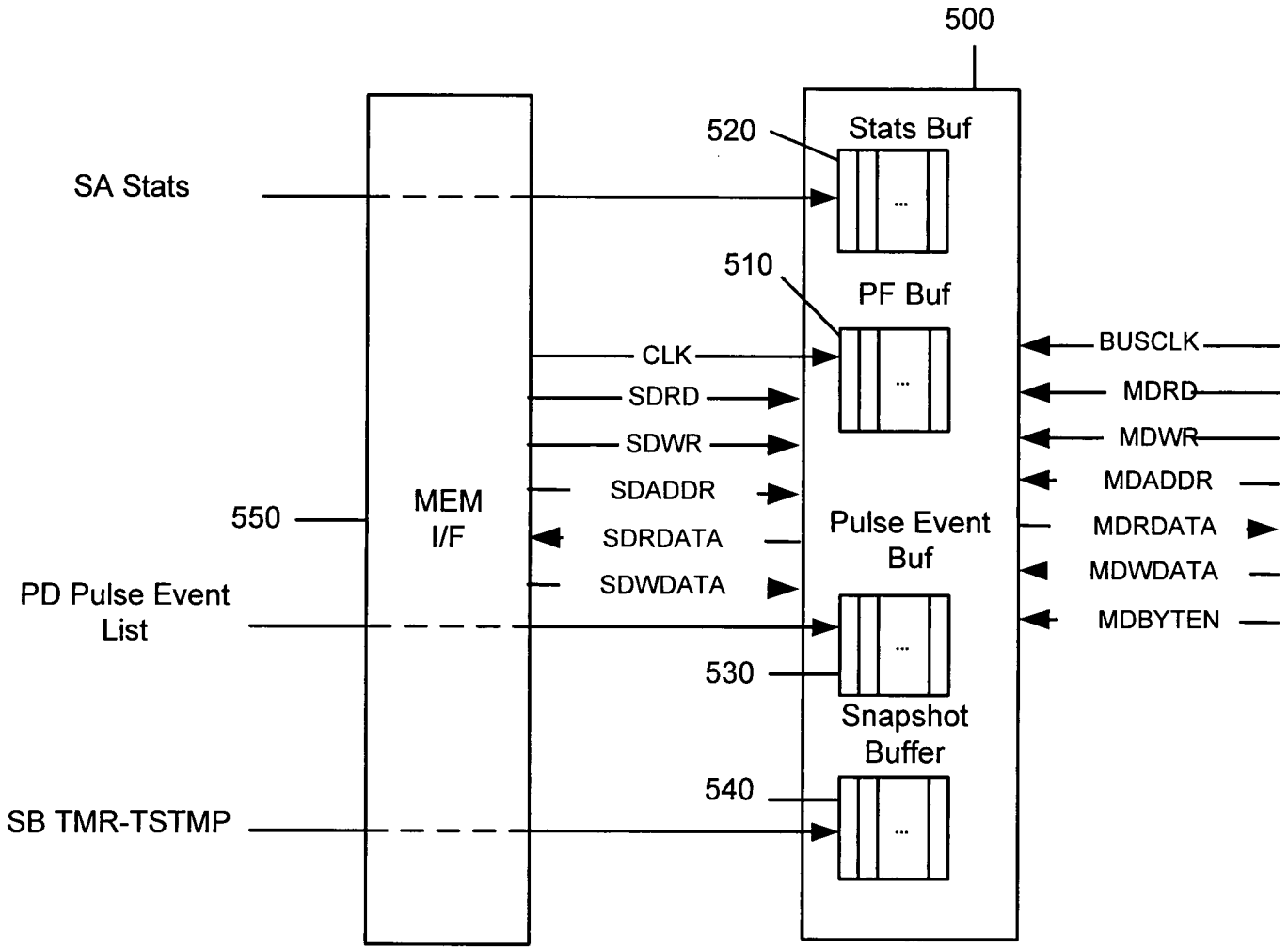

500
520
Stats Buf
SA Stats
510
PF Buf
CLK
SDRD
SDWR
SDADDR
SDRDATA
SDWDATA
550
MEM
I/F
Pulse Event
Buf
PD Pulse Event
List
530
Snapshot
Buffer
540
SB TMR-TSTMP
BUSCLK
MDRD
MDWR
MDADDR
MDRDATA
MDWDATA
MDBYTEN

FIG. 14

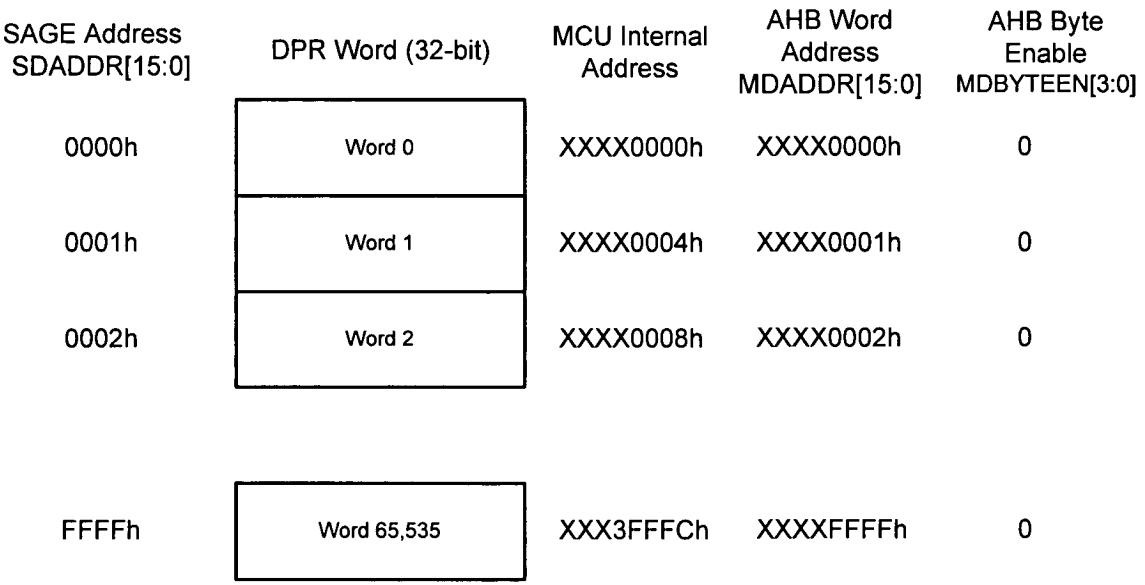

SAGE Address SDADDR[15:0]
DPR Word (32-bit)
MCU Internal Address
AHB Word Address MDADDR[15:0]
AHB Byte Enable MDBYTEEN[3:0]
0000h
Word 0
XXXX0000h
XXXX0000h
0
0001h
Word 1
XXXX0004h
XXXX0001h
0
0002h
Word 2
XXXX0008h
XXXX0002h
0
FFFFh
Word 65,535
XXX3FFFCh
XXXXFFFFh
0

FIG. 15

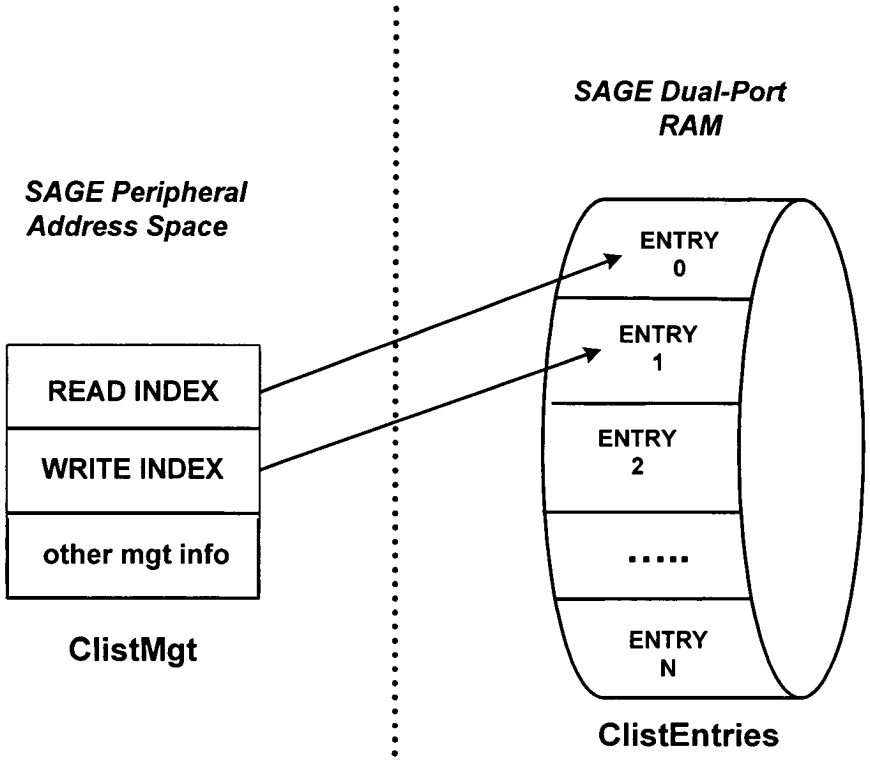

SAGE Dual-Port RAM
SAGE Peripheral Address Space
READ INDEX
WRITE INDEX
other mgt info
ClistMgt
ENTRY 0
ENTRY 1
ENTRY 2
.....
ENTRY N
ClistEntries

FIG. 16

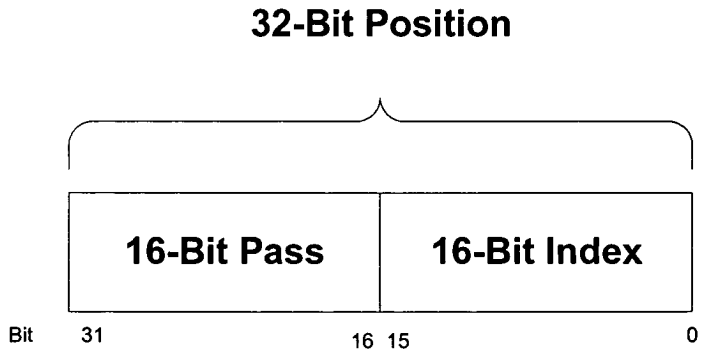

32-Bit Position
16-Bit Pass
16-Bit Index
Bit
31
16
15
0

FIG. 17

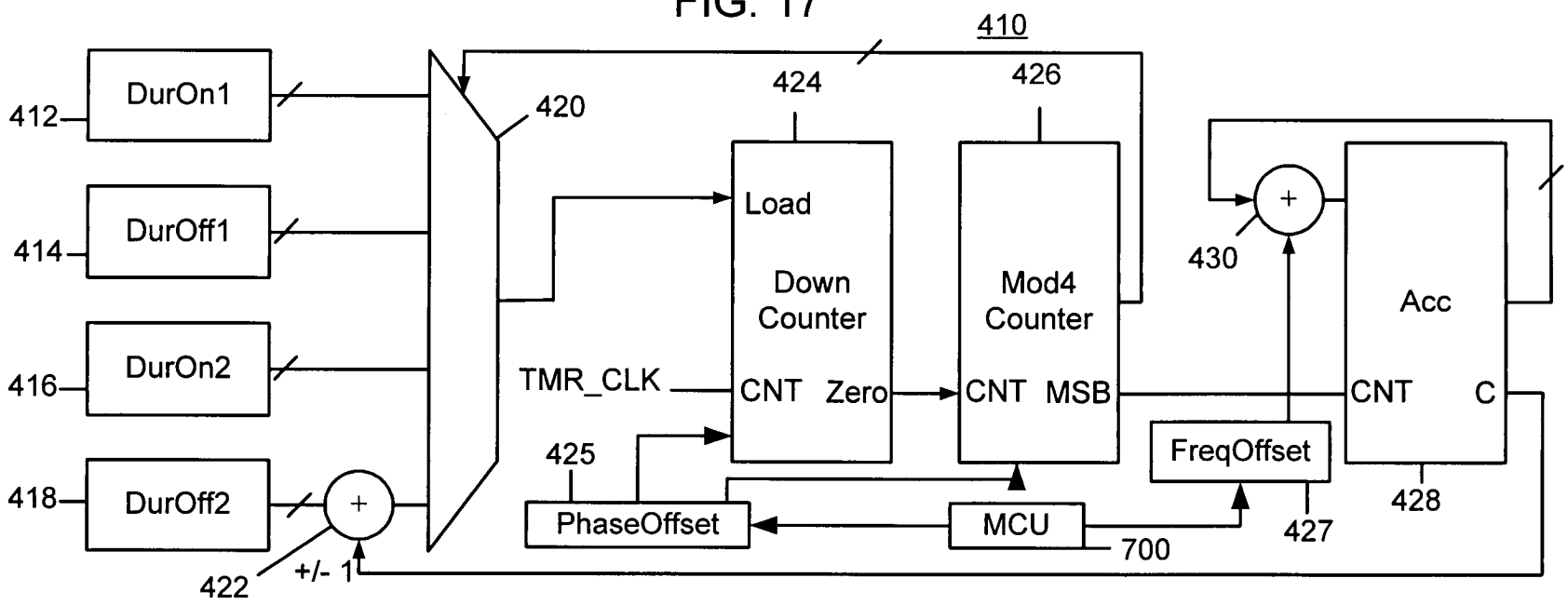

410
412
DurOn1
414
DurOff1
416
DurOn2
418
DurOff2
422
+/- 1
420
424
426
Load
Down Counter
CNT Zero
TMR_CLK
425
PhaseOffset
Mod4 Counter
CNT MSB
MCU
700
430
FreqOffset
427
Acc
CNT C
428

FIG. 18

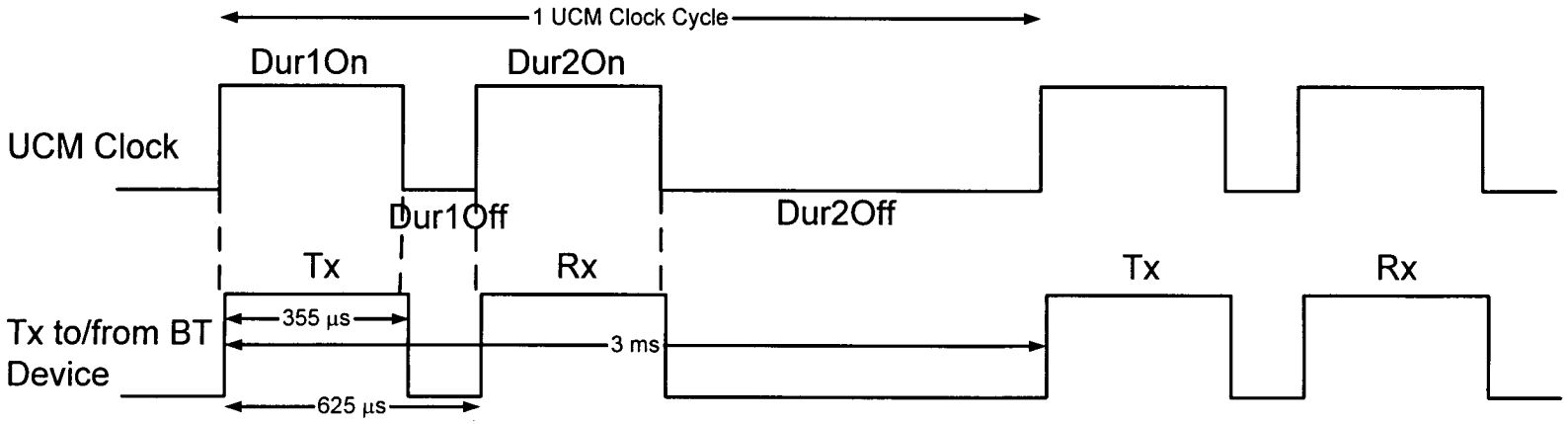

1 UCM Clock Cycle
Dur1On
Dur2On
UCM Clock
Dur1Off
Dur2Off
Tx
Rx
Tx
Rx
Tx to/from BT Device
355 µs
3 ms
625 µs

FIG. 19

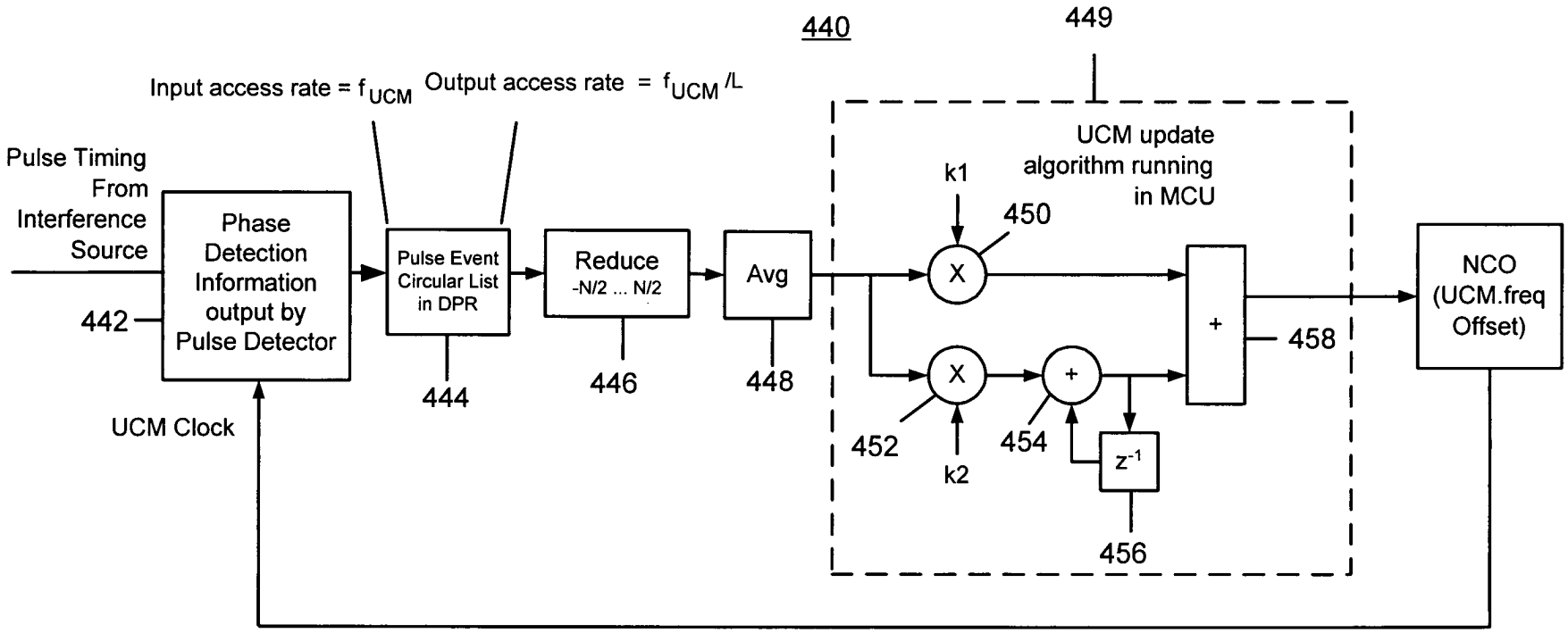

440
449
Input access rate = f_{UCM}
Output access rate = f_{UCM} /L
Pulse Timing From Interference Source
442
Phase Detection Information output by Pulse Detector
UCM Clock
Pulse Event Circular List in DPR
444
Reduce -N/2 ... N/2
446
Avg
448
UCM update algorithm running in MCU
k1
450
X
X
k2
452
+
454
z^{-1}
456
+
458
NCO (UCM.freq Offset)

FIG. 20

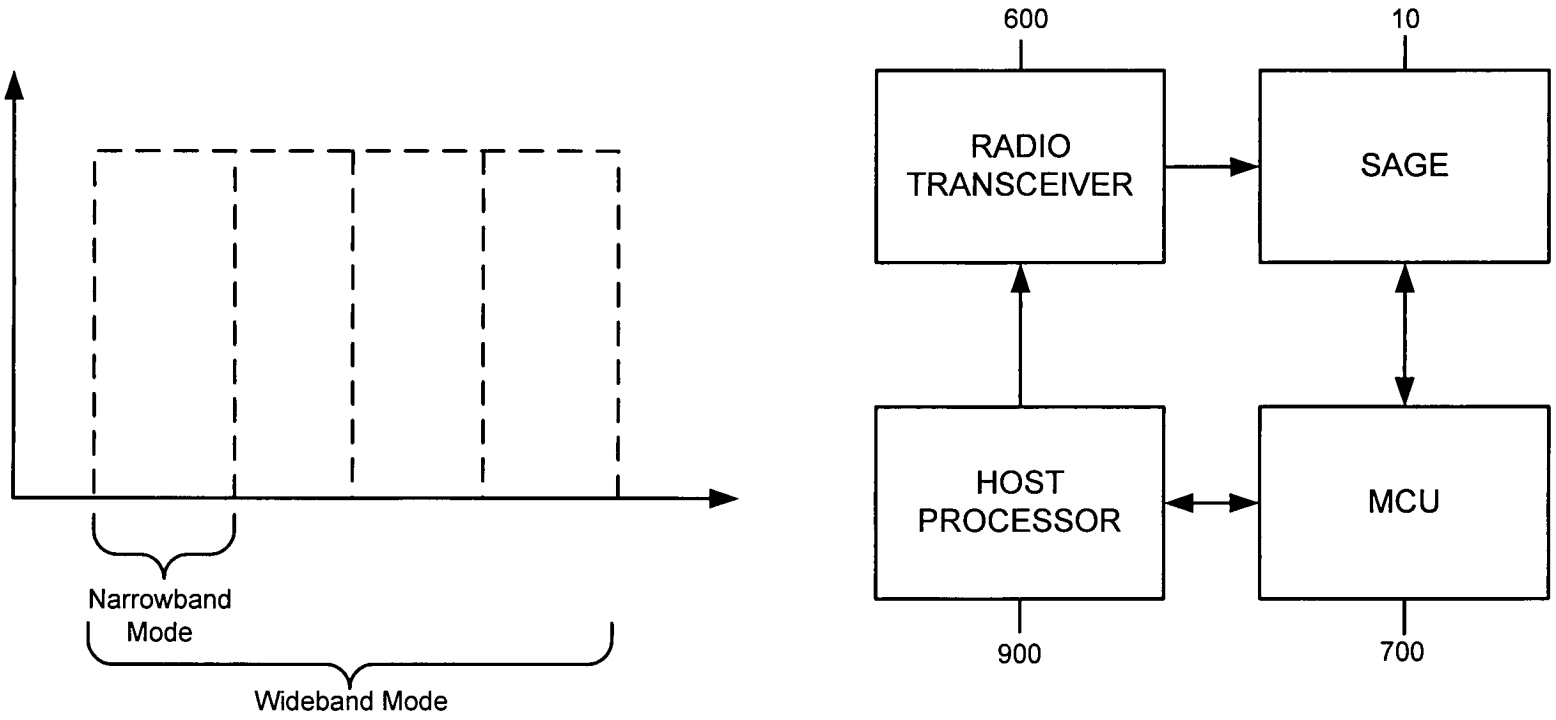

Narrowband Mode
Wideband Mode
600
10
RADIO TRANSCEIVER
SAGE
HOST PROCESSOR
MCU
900
700

FIG. 21

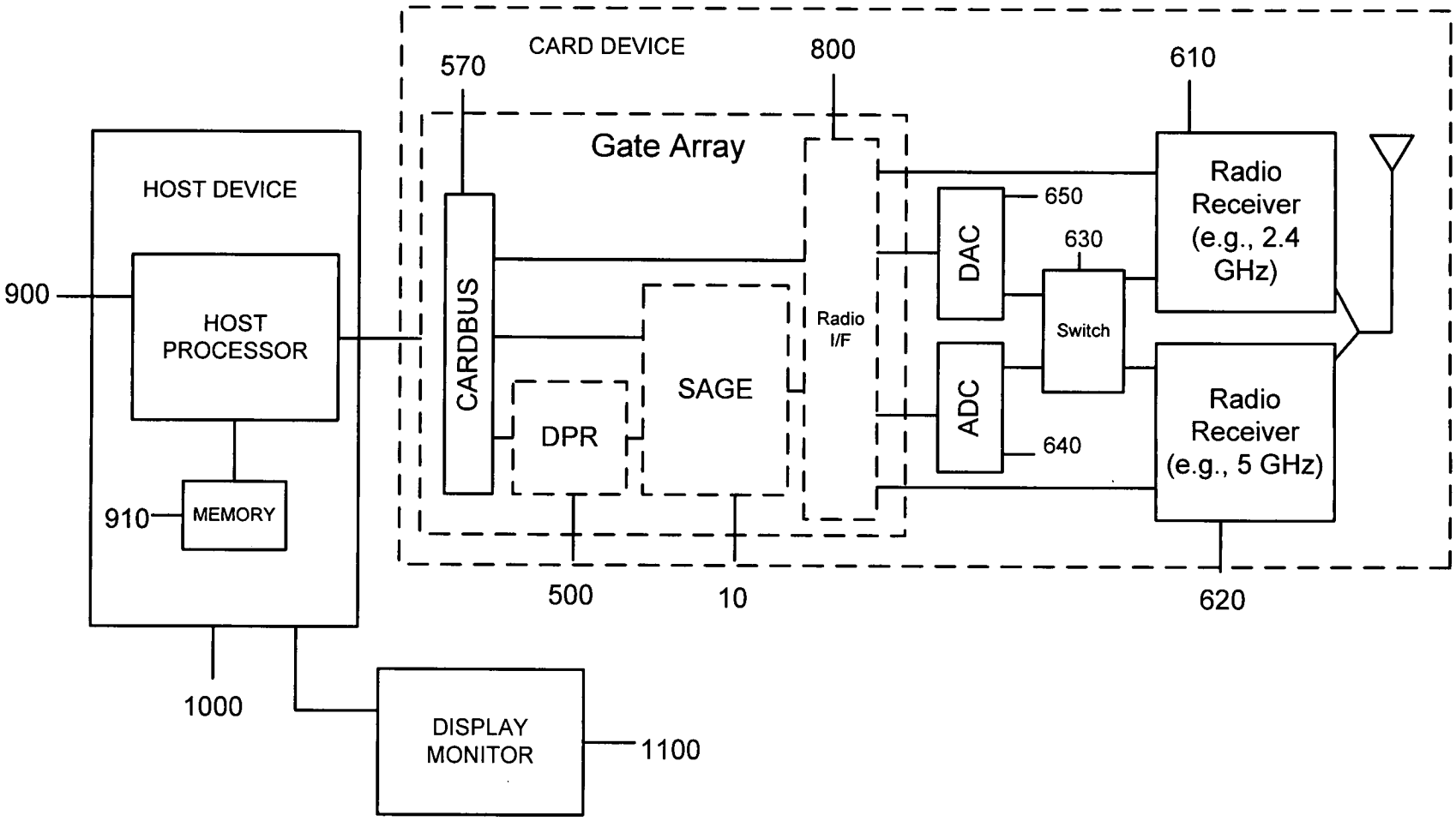
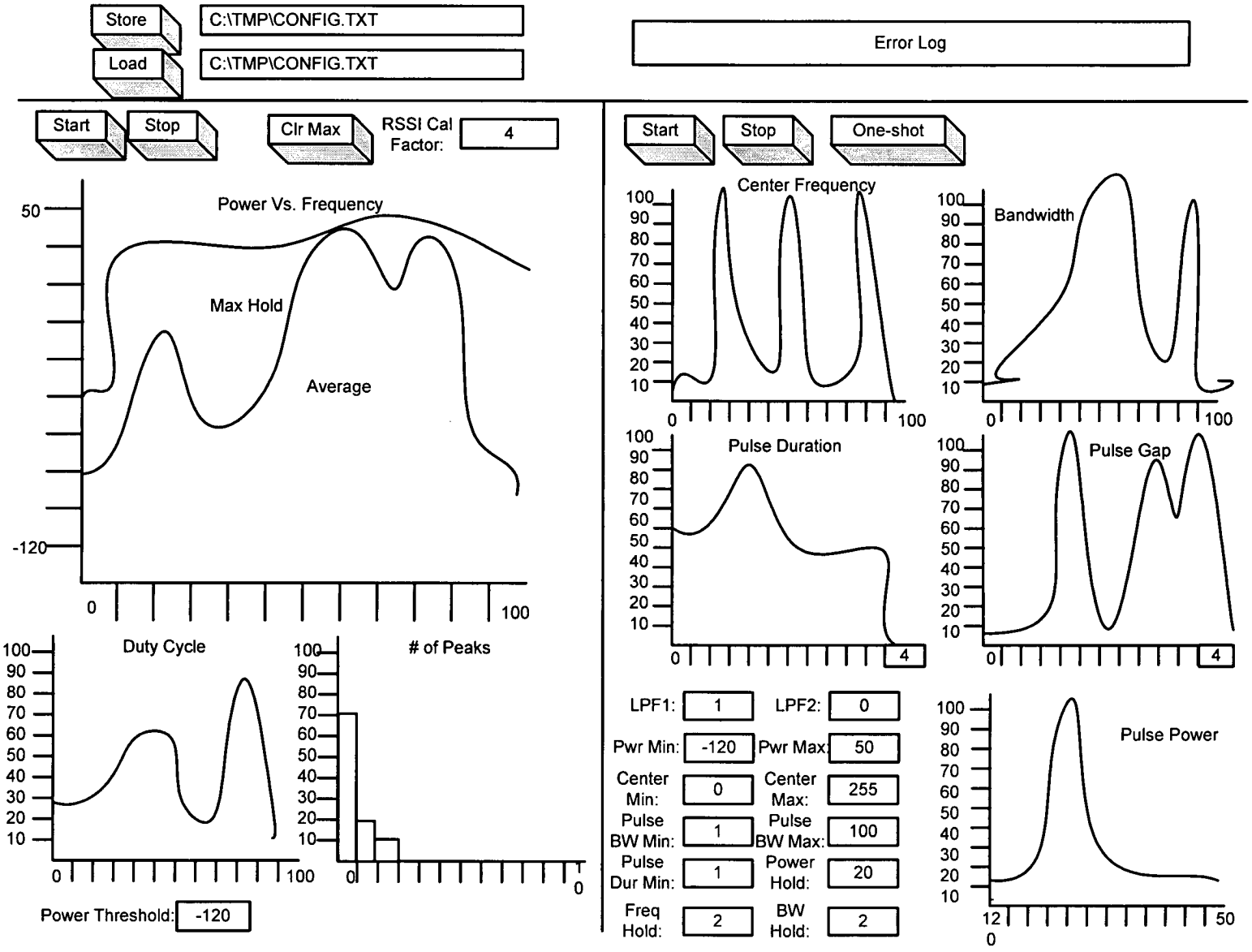

CARD DEVICE
570
800
610
Gate Array
HOST DEVICE
900
HOST PROCESSOR
910
MEMORY
1000
CARDBUS
DPR
SAGE
Radio I/F
DAC
650
630
Switch
ADC
640
Radio Receiver (e.g., 2.4 GHz)
Radio Receiver (e.g., 5 GHz)
500
10
620
DISPLAY MONITOR
1100

FIG. 22


Store
C:\TMP\CONFIG.TXT
Load
C:\TMP\CONFIG.TXT
Error Log
Start
Stop
Clr Max
RSSI Cal Factor:
4
Power Vs. Frequency
Max Hold
Average
50
-120
0
100
Duty Cycle
# of Peaks
Power Threshold:
-120
Start
Stop
One-shot
Center Frequency
Bandwidth
Pulse Duration
Pulse Gap
Pulse Power
LPF1:
1
LPF2:
0
Pwr Min:
-120
Pwr Max:
50
Center Min:
0
Center Max:
255
Pulse BW Min:
1
Pulse BW Max:
100
Pulse Dur Min:
1
Power Hold:
20
Freq Hold:
2
BW Hold:
2